AGENDA

1. Introduction to HDI
2. Using HDI in circuit design
3. Use of HDI in a project
4. Lessons learned
5. Conclusion
What is HDI?

• High Density Interconnect
• Advanced PCB technology
• Simply put:
  o Smaller vias, both blind and buried
  o Smaller traces
• Can reduce PCB area and layers needed
• More reliable
• Becoming more cost effective

From the HDI Handbook
History of HDI

- HP FINSTRATE (1984) 32-bit computer
- 1990s
- Used in early Sony camcorders (1996)
- Rapid growth from 2000
Related IPC standards

- **IPC/JPCA-2315**: Design Guide for High-density Interconnect Structures and Microvias
- **IPC-2226**: Sectional Design Standard for High-density Interconnect (HDI) Printed Boards
- **IPC/JPCA-4104**: Qualification and Performance Specification for Dielectric Materials for High-density Interconnect Structures (HDI)
- **IPC-6016**: Qualification and Performance Specification for High-density Interconnect (HDI) Structures
IPC-2226 Definition of HDI

- PCB with finer lines and spaces ≤ 100 um
- Vias are ≤ 150 um and capture pads are < 400 um
- Higher connection pad density than conventional PCB (>20 pads/cm^2)
IPC-2226 Definition of Microvia

- Has a capture pad diameter ≤ 350 um
- Has a plated hole with a diameter ≤ 150 um formed either by laser or mechanical drilling
- Hole with an aspect ratio of 1:1 (normal PTH typically 10:1)
Via types

- Plated through hole via (PTH): Outer layer to outer layer
- Blind via: Outer layer to inner layer
- Buried via: Inner layer to inner layer
- Microvias
Via aspect ratio (AR)

- Defined as the relationship between the diameter of the hole and its length.
- Usually in the range of 6:1 to 10:1 for PTH
- 10:1 is the minimum for PTH (lower reliability)
- 6:1 recommended for highest reliability
- Thicker board = larger vias
Microvias

- AR of 1:1 / 1:0.8
- Staggered
- Copper filled (via-in-pad)
- Stacked
- Skip
- Buried

From Interrupt Inside: High Density Interconnect - Haldor Husby
HDI PCB Fabrication process

Core -> Etch

Hot pressed together
(copper + Inner board + PP + copper) Lamination become core

Buried vias filled->

Drill 2

Laser drill 1

PTH/PP2

Lamination 2

Inner 2
PCB fabrication costs

- Blind Vias (+20% to +40% fabrication cost)
- Buried Vias (+25% to +60% fabrication cost)
- Micro Vias (+30% fabrication cost)
- Back-drilled Vias (+10% fabrication cost)
- Via-In-Pad (+30% fabrication cost)
- Extra Layers (+20% fabrication cost (per every two layers))

Cost estimates from Xilinx
IPC-2226 HDI Type I and II

- Type I: One HDI layer on top and/or bottom with through-vias from surface to surface.
- Type II: One HDI layer on top and/or bottom with buried vias in the core and may have through-vias connecting the outer layers from surface to surface.
IPC-2226 HDI Type III

- Most used type
- Two or more HDI layers added to through-vias in the core or from surface to surface
- Buried vias
- Stacked microvias
- Used on the project described in this presentation
IPC-2226 HDI Type IV, V and VI

- Less used
- Type IV: Passive core substrate with no electrical connecting functions.
- Type V: Coreless constructions using layer pairs.
- Type VI: Alternate constructions of coreless construction using layer pairs.
BGA breakout aspects

• Route density
• Cost
• Signal Integrity
• Power Integrity
Breakout patterns

- Adjacent (dog-bone)
- Partial via-in-pad
- Via-in-pad (centered)
**PTH vs Microvia breakout**

- Smaller capture pad
- Routing of multiple traces
- 10:1 vs 1:0.8 AR

From *Interrupt Inside: High Density Interconnect* - Haldor Husby

From IPC-2226
How many signal layers are needed?

BGA Pitch 0.8mm - 20 x 20 rows

Standard PTH, dogbone technique

“Dogbone” fan out

From the Wurth HDI Webinar
How many signal layers are needed?

BGA Pitch 0.8mm - 20 x 20 rows

Microvia, via in pad allows two tracks between the vias

Note: Example above requires stacked microvias, which adds some additional cost and affects overall reliability

From the Wurth HDI Webinar
Not just for BGA...

QFN with PTH

QFN with Microvia (via in pad)

From the Wurth HDI Webinar
High speed / signal integrity

- HDI instead of expensive high frequency material
- Via in pads, shorter trace lengths
- Remove via stubs
- Avoid backdrilling of vias

From the Wurth HDI Webinar
Reliability

- Vias especially important
- Ranked most robust to least:
  1. Micro via
  2. Staggered microvia
  3. Through hole via
  4. Stacked microvia
  5. Blind via
  6. Buried via

Thermal expansion of PCB material (ie during reflow) ->

From Haldor Husby Reliability presentation
Via-in-pad filling

- Gassing during reflow caused by an unfilled via-in-pad, causing excessive package movement
- Can be prevented by precise control of flux/solder paste and reflow temperature profile
- Or by copper/epoxy filling (extra cost)
Acoustic sensor project

- Acoustic data measurement
- Record and store acoustic data through multiple sensors
- Continuous operation for several weeks
- Several terabytes of data
- Schematic by Data Respons, PCB layout by Asian company
Functional block diagram

- Acoustic Data Collection module
- Xilinx Ultrascale SoC
- 32 transducers
- LPDDR4
- eMMC, QSPI
- Ethernet, PCIe
Proposed floorplan

- 110mm x 250 mm
- ~5000 components
- Very high density board
- Big challenge for Asian company
PCB Specifications

- 14 layer
- FR-4
- L1-L2 & L2-L3 and symmetric on bottom layers.
- Type III HDI
- No stacked microvia or microvia on buried via (reliability)
- Outer vias filled and capped (allows via-in-pad)
- Buried microvias not filled or capped
SoC BGA Breakout

- 0.8mm pitch
- 28x28, 784 pin BGA
- Ground and VCC pins sprinkled around
PCB layout process

- Communication primarily through Confluence
- No direct contact with PCB manufacturer
- NCAB HDI PCB design rules
- Language barrier
- Layout comments in Confluence
- BGA breakout mix of via-in-pad and buried vias
- Overworked layout designers

Top Layer

Layer 3

Layer 4
Asian PCB manufacturing issues

- Chinese HDI manufacturers overloaded (bitcoin craze)
- Small prototype runs was a low priority
- 5 weeks lead time
- Failed to meet the required 10% accuracy of impedance
- All boards scrapped without question...
NCAB manufacturing issues

- European (Macedonia) vendor
- ~10 days production time
- Fault in the final step of the manufacturing process
- Wrong parameters on the laser drilling of the microvias caused short circuits between layers
- Even when following NCABs own design rules, the manufacturing process still failed
- Second attempt succeeded
Lessons learned

• PCB manufacturing capabilities needed
• Running dialog with layout designer and PCB manufacturer is vital
• Dense and complex PCB, but in theory not difficult to produce
• Even fairly conservative designs can fail
• The HDI standard is not yet standard
• Each manufacturer have their own processes
Conclusion

• The HDI process is under development
• Close cooperation between schematic designer, layout designer and PCB manufacturer is needed to decrease cost and improve reliability
Recommended reading

• The HDI Handbook - Happy Holden et. al
• HDI Webinars - Wurth
• BGA Breakouts and Routing - Charles Pfeil
• HDI Design Guidelines - NCAB
• HDI Layer Stackups for Large Dense PCBs - Happy Holden & Charles Pfeil
• IPC-2226 and other HDI related IPC standards
0.5mm, 0.4mm, 0.3mm...

0.4mm is becoming more and more common, with 0.3mm on the horizon
(0.3mm already used in telecom industry...)

0402 footprint ->
Smartphone trend

Iphone 1 (2007)

Iphone X (2018)
Sources

- Iphone 1 vs Iphone X: [https://www.idownloadblog.com/2017/11/03/gallery-iphone-x-original-iphone/](https://www.idownloadblog.com/2017/11/03/gallery-iphone-x-original-iphone/)
- 0.3mm BGA pitch: [https://www.hotwires.net/?tag=0-3mm-bga](https://www.hotwires.net/?tag=0-3mm-bga)
- Via types: [https://www.allpcb.com/pcb/vias.html](https://www.allpcb.com/pcb/vias.html)
- HDI in the Iphone X: [https://www.macrumors.com/2017/11/02/fight-for-space-iphone-x/](https://www.macrumors.com/2017/11/02/fight-for-space-iphone-x/)
- A11 InFO stacked chip: [https://wccftech.com/apple-a10-die-shots-chipworks-iphone-7/](https://wccftech.com/apple-a10-die-shots-chipworks-iphone-7/)
Questions?
A smarter solution starts from inside

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